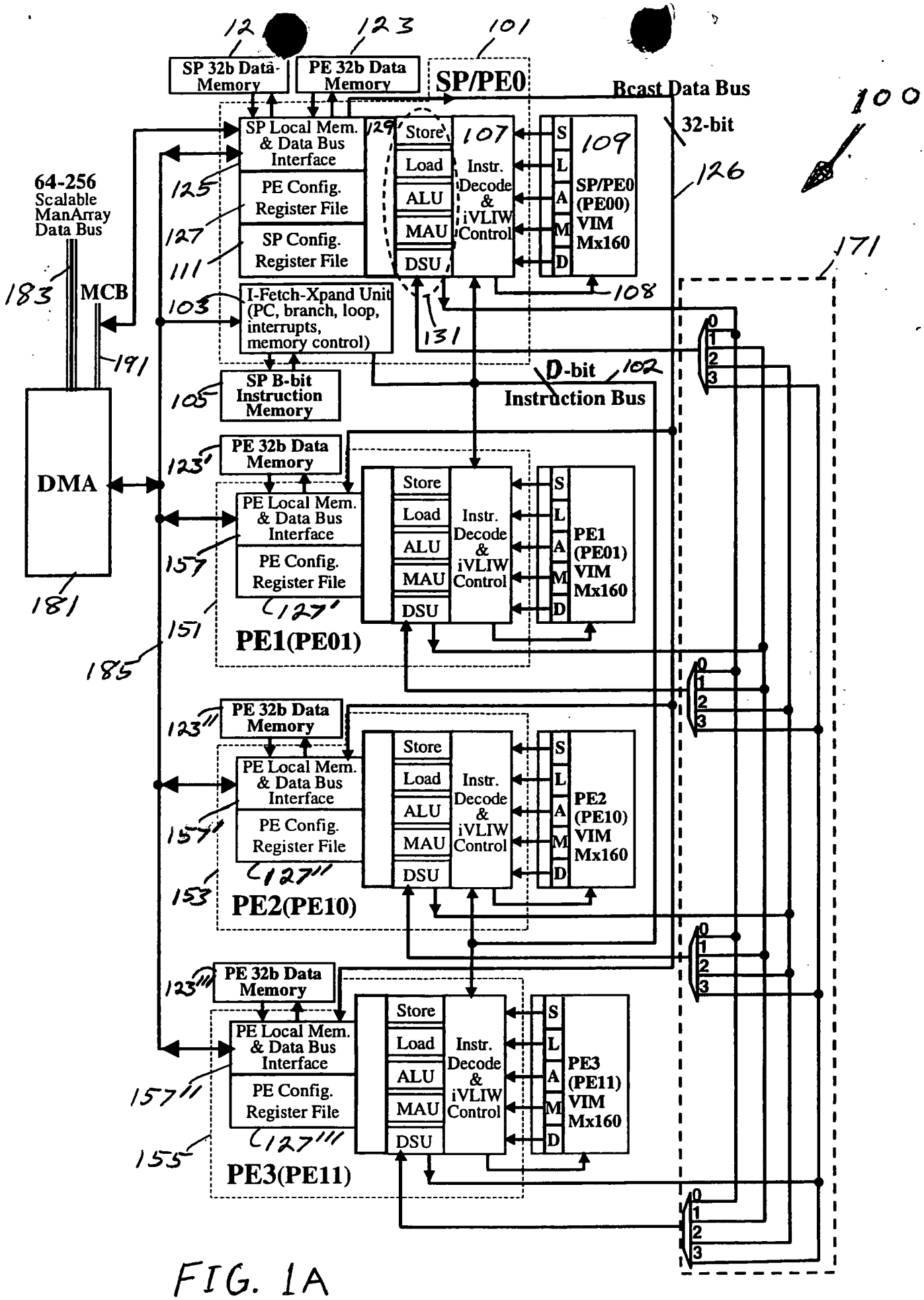
SP 32b Data Memory
PE 32b Data Memory
SP/PE0
Bcast Data Bus
32-bit
100
SP Local Mem. & Data Bus Interface
PE Config. Register File
SP Config. Register File
Store
Load
ALU
MAU
DSU
Instr. Decode & iVLIW Control
S
L
A
M
D
SP/PE0 (PE00) VIM Mx160
64-256 Scalable ManArray Data Bus
MCB
I-Fetch-Xpand Unit (PC, branch, loop, interrupts, memory control)
SP B-bit Instruction Memory
D-bit Instruction Bus
DMA
PE 32b Data Memory
PE Local Mem. & Data Bus Interface
PE Config. Register File
PE1 (PE01) VIM Mx160
PE1(PE01)
PE2 (PE10) VIM Mx160
PE2(PE10)
PE3 (PE11) VIM Mx160
PE3(PE11)
0
1
2
3

FIG. 1A

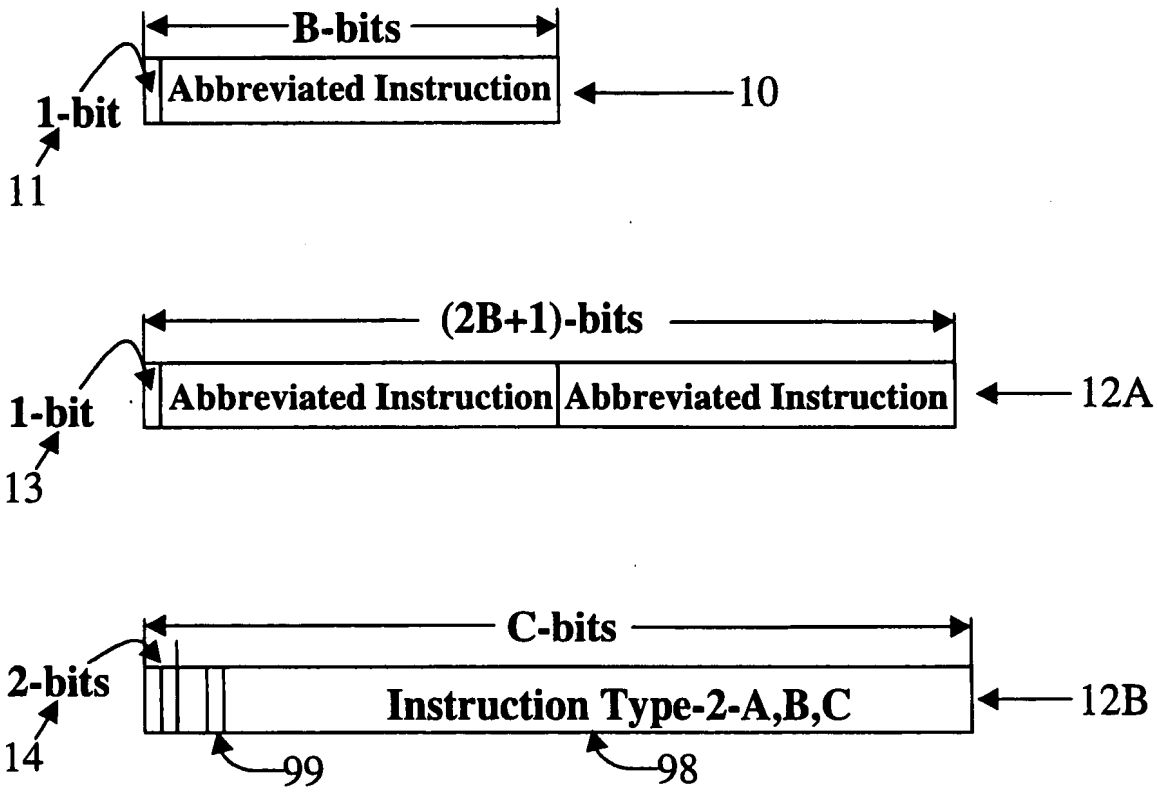
B-bits
Abbreviated Instruction
10
1-bit
11
(2B+1)-bits
Abbreviated Instruction
Abbreviated Instruction
12A
1-bit
13
C-bits
Instruction Type-2-A,B,C
12B
2-bits
14
99
98

FIG. 1B

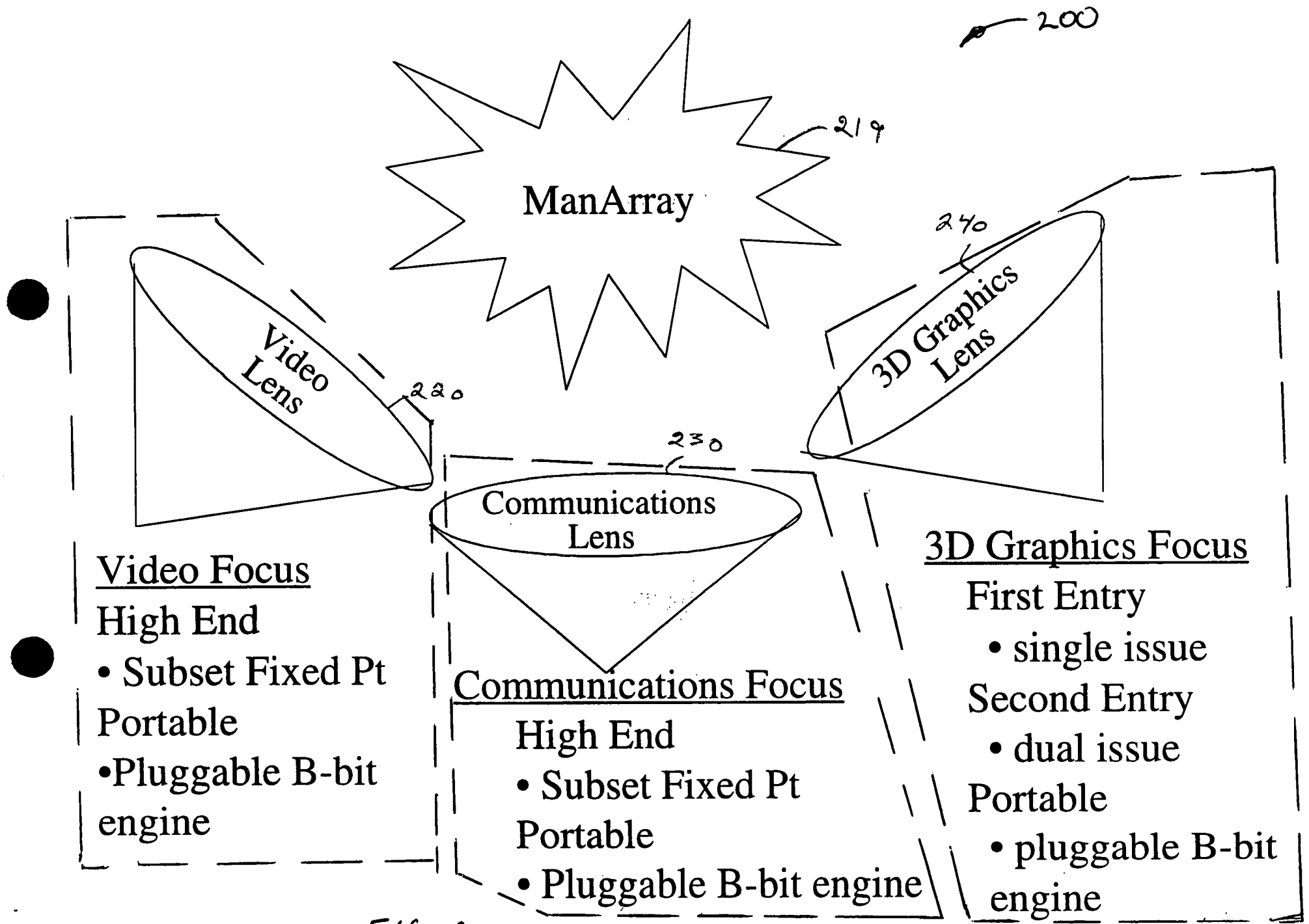
200
219
ManArray
240
3D Graphics Lens
Video Lens
220
230
Communications Lens
Video Focus
High End
• Subset Fixed Pt
Portable
•Pluggable B-bit engine
Communications Focus
High End
• Subset Fixed Pt
Portable
• Pluggable B-bit engine
3D Graphics Focus
First Entry
• single issue
Second Entry
• dual issue
Portable
• pluggable B-bit engine

FIG. 2

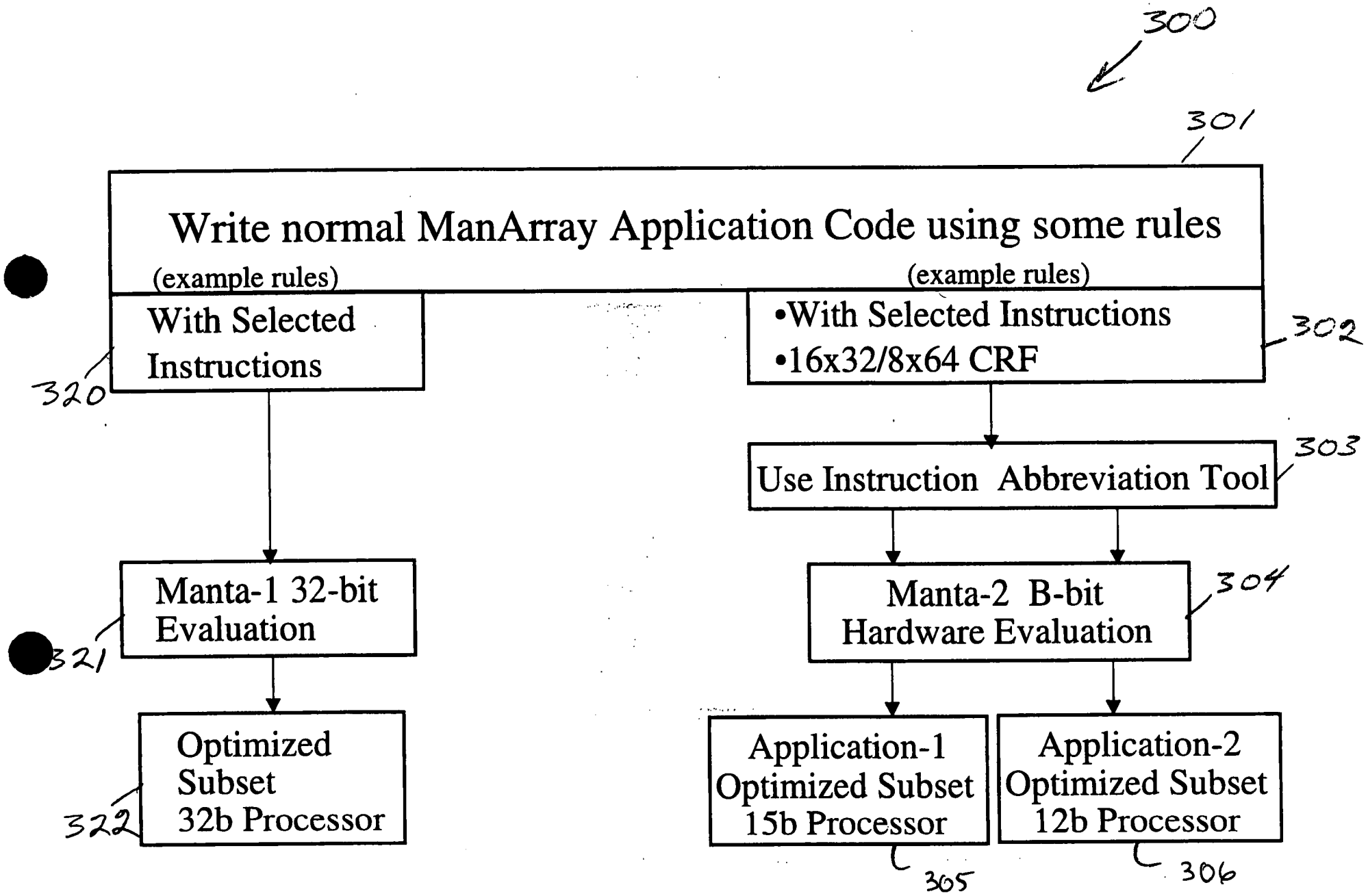

FIG. 3A

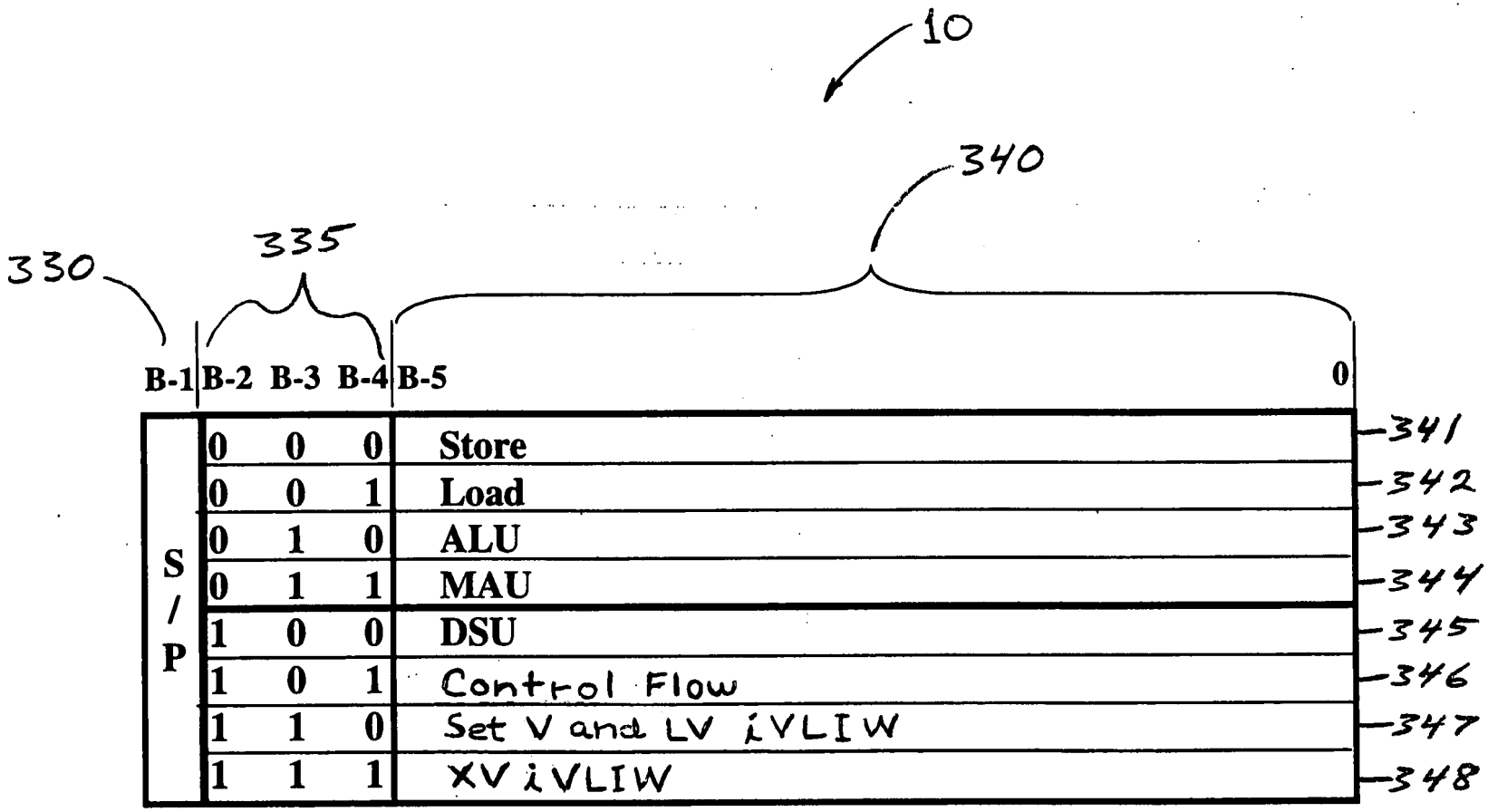
10
340
335
330
B-1
B-2 B-3 B-4
B-5
0
S / P
0 0 0 Store
0 0 1 Load
0 1 0 ALU
0 1 1 MAU
1 0 0 DSU
1 0 1 Control Flow
1 1 0 Set V and LV iVLIW
1 1 1 XV iVLIW
341
342
343
344
345
346
347
348

FIG. 3B

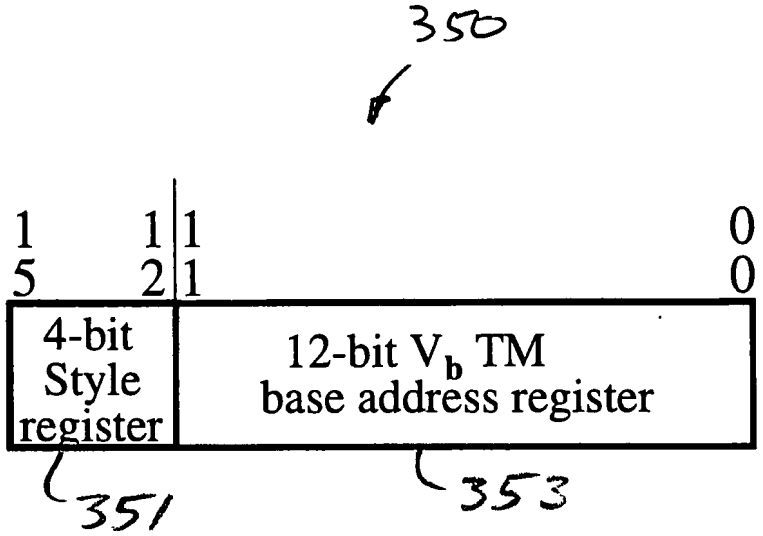

FIG. 3C

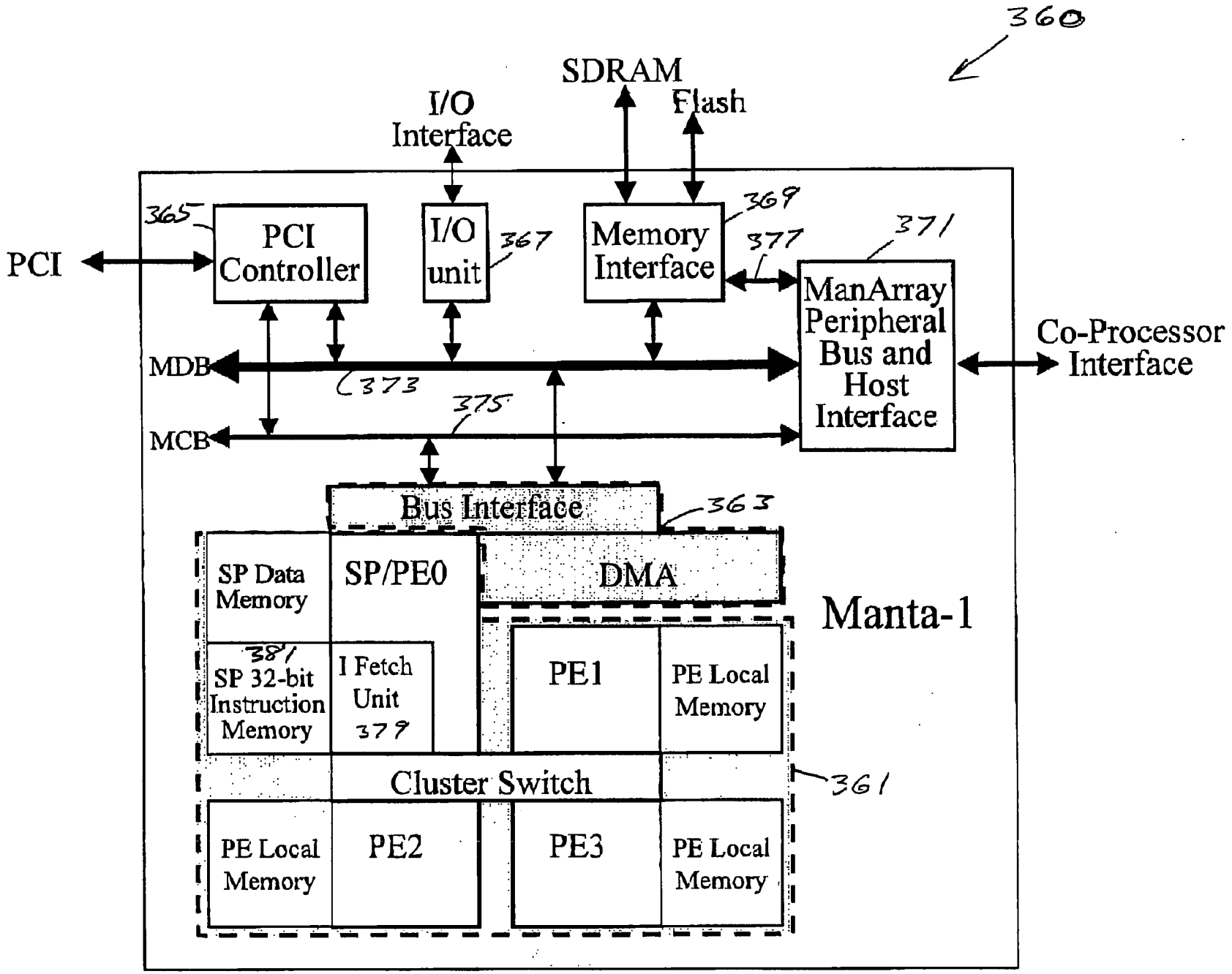
360
SDRAM
Flash
I/O Interface
PCI
PCI Controller
365
I/O unit
367
Memory Interface
369
377
371
ManArray Peripheral Bus and Host Interface
Co-Processor Interface
MDB
373
375
MCB
Bus Interface
363
SP Data Memory
SP/PE0
DMA
Manta-1
381
SP 32-bit Instruction Memory
I Fetch Unit
379
PE1
PE Local Memory
Cluster Switch
361
PE Local Memory
PE2
PE3
PE Local Memory

FIG. 3D

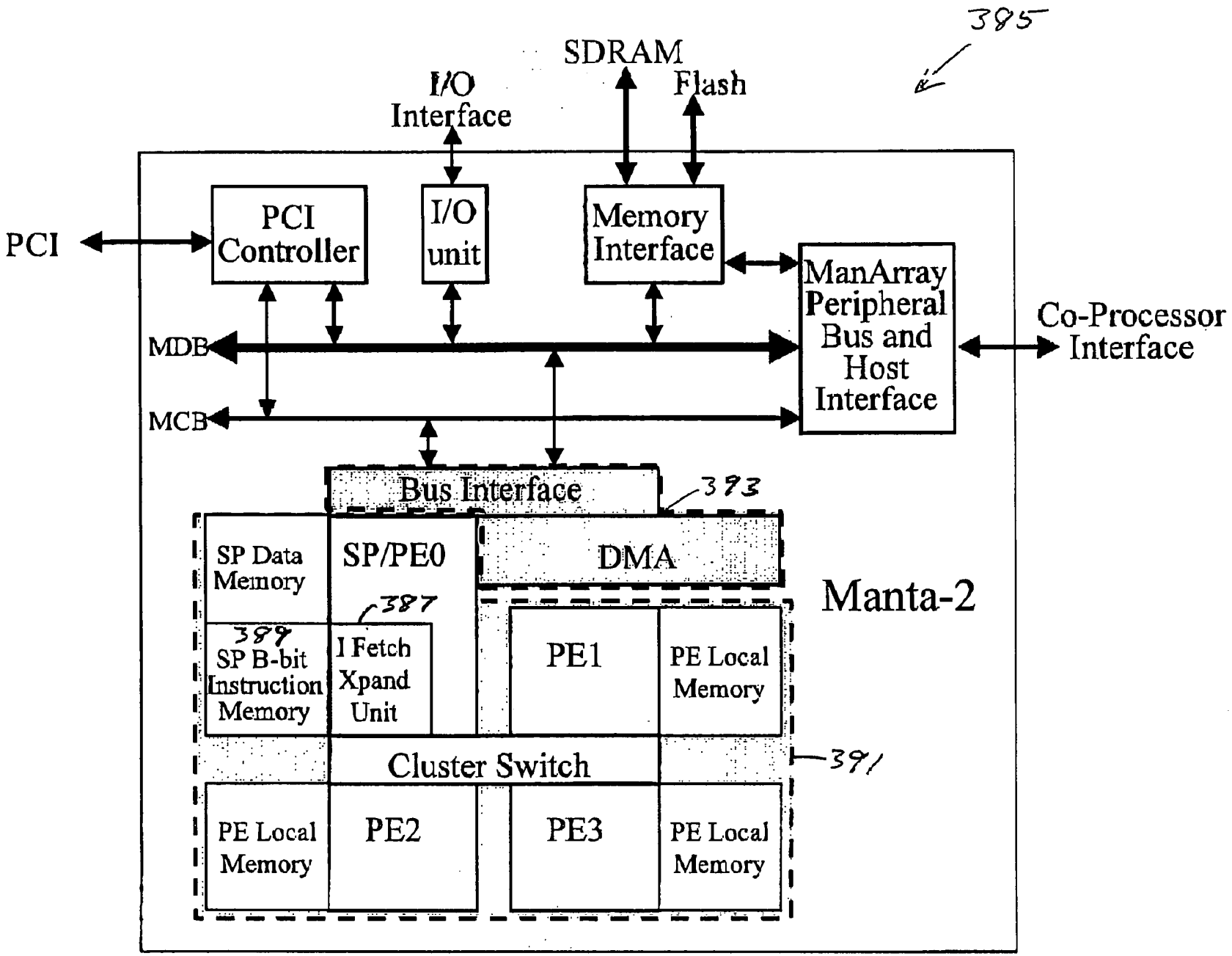
385
SDRAM
Flash
I/O
Interface
PCI
PCI
Controller
I/O
unit
Memory
Interface
ManArray
Peripheral
Bus and
Host
Interface
Co-Processor
Interface
MDB
MCB
Bus Interface
393
SP Data
Memory
SP/PE0
DMA
387
389
SP B-bit
Instruction
Memory
I Fetch
Xpand
Unit
PE1
PE Local
Memory
Manta-2
Cluster Switch
391
PE Local
Memory
PE2
PE3
PE Local
Memory

FIG. 3E

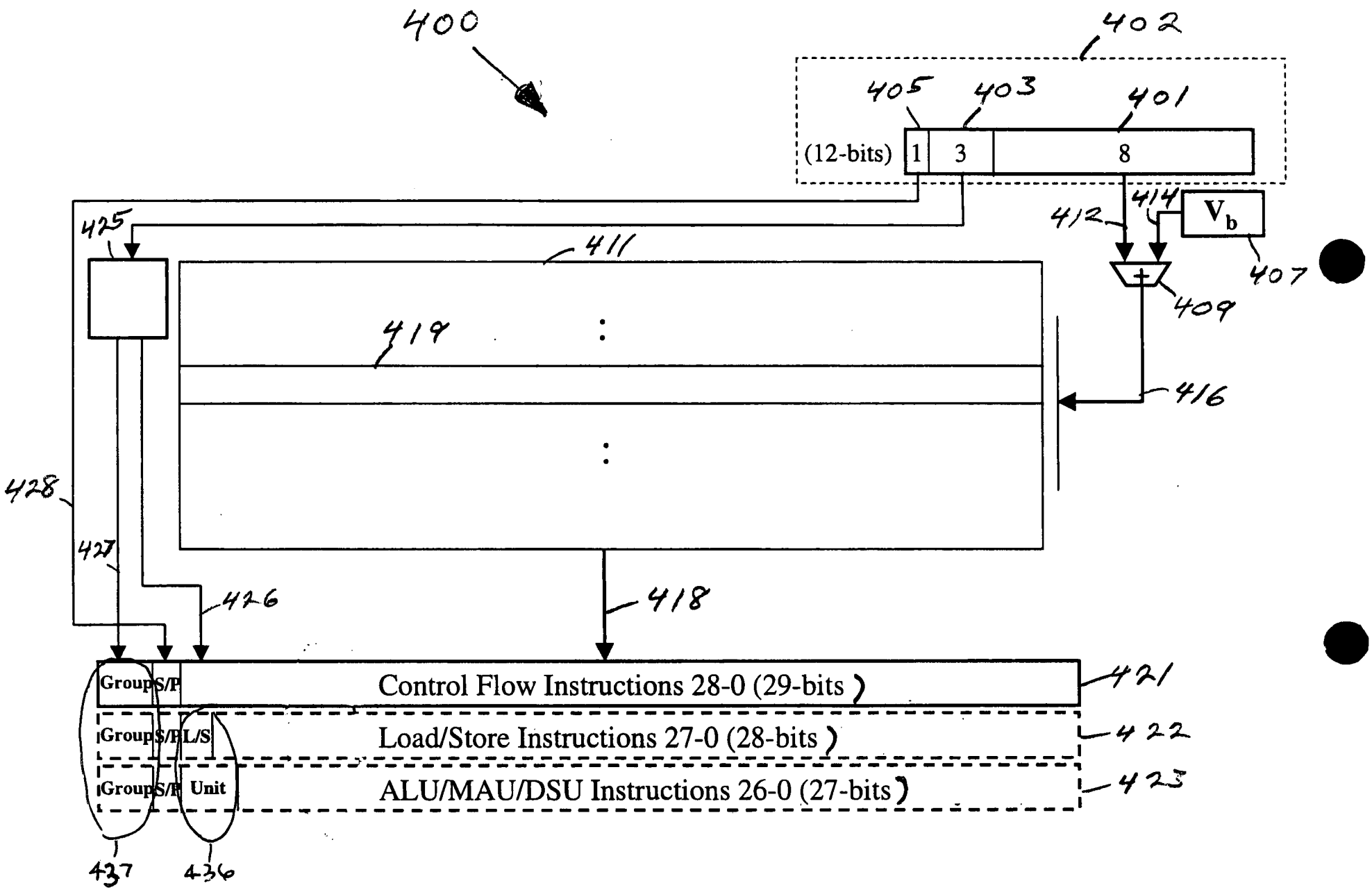
400
402
405
403
401
(12-bits)
1
3
8
414
V_b
412
407
409
425
411
419
416
428
427
426
418
Group
S/P
Control Flow Instructions 28-0 (29-bits)
421
Group
S/P
L/S
Load/Store Instructions 27-0 (28-bits)
422
Group
S/P
Unit
ALU/MAU/DSU Instructions 26-0 (27-bits)
423
437
436

Fig. 4

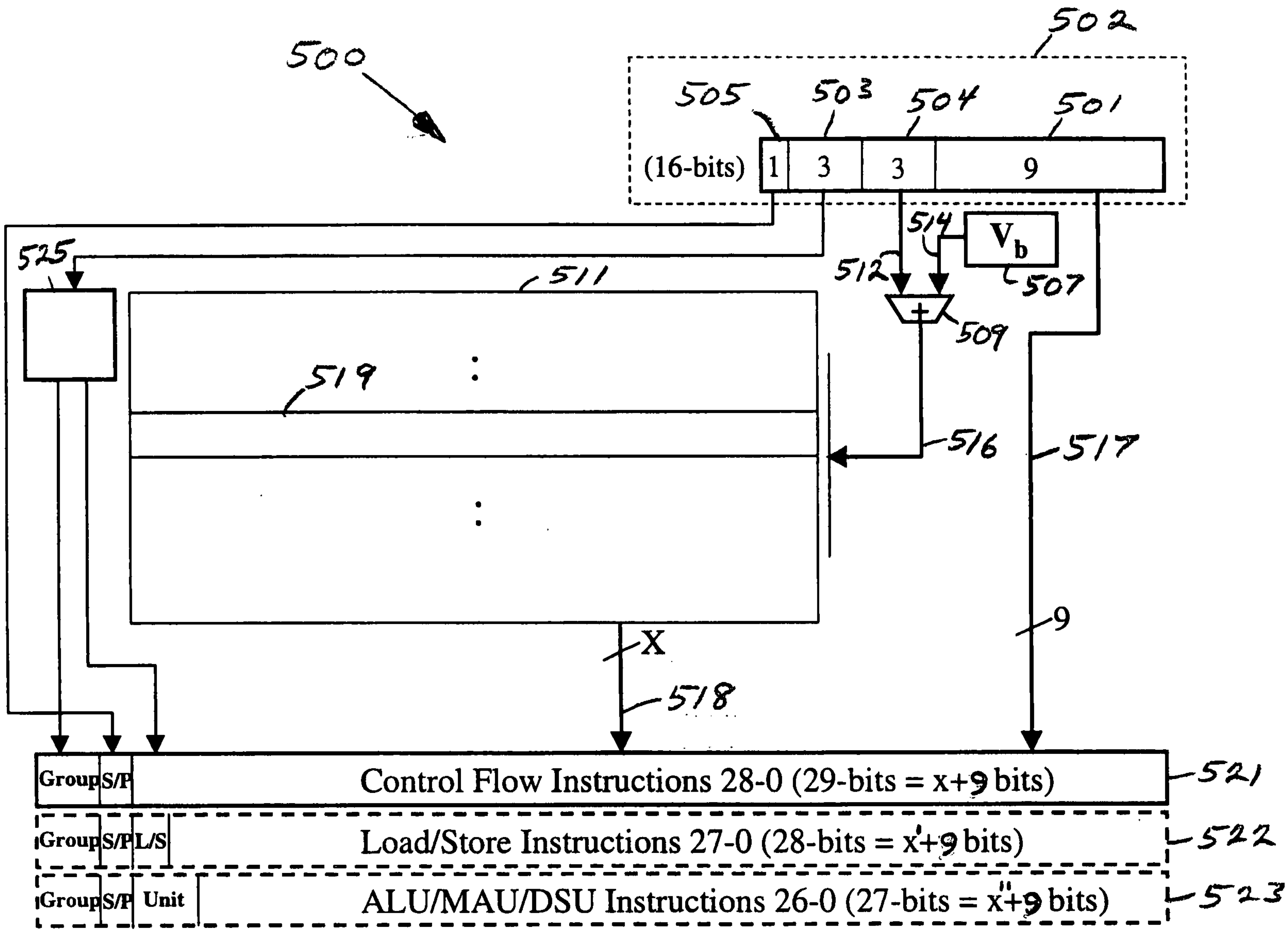
500
502
505
503
504
501
(16-bits)
1
3
3
9
514
Vb
512
507
509
525
511
519
516
517
9
X
518
Group
S/P
Control Flow Instructions 28-0 (29-bits = x+9 bits)
521
Group
S/P
L/S
Load/Store Instructions 27-0 (28-bits = x'+9 bits)
522
Group
S/P
Unit
ALU/MAU/DSU Instructions 26-0 (27-bits = x''+9 bits)
523

Fig. 5A

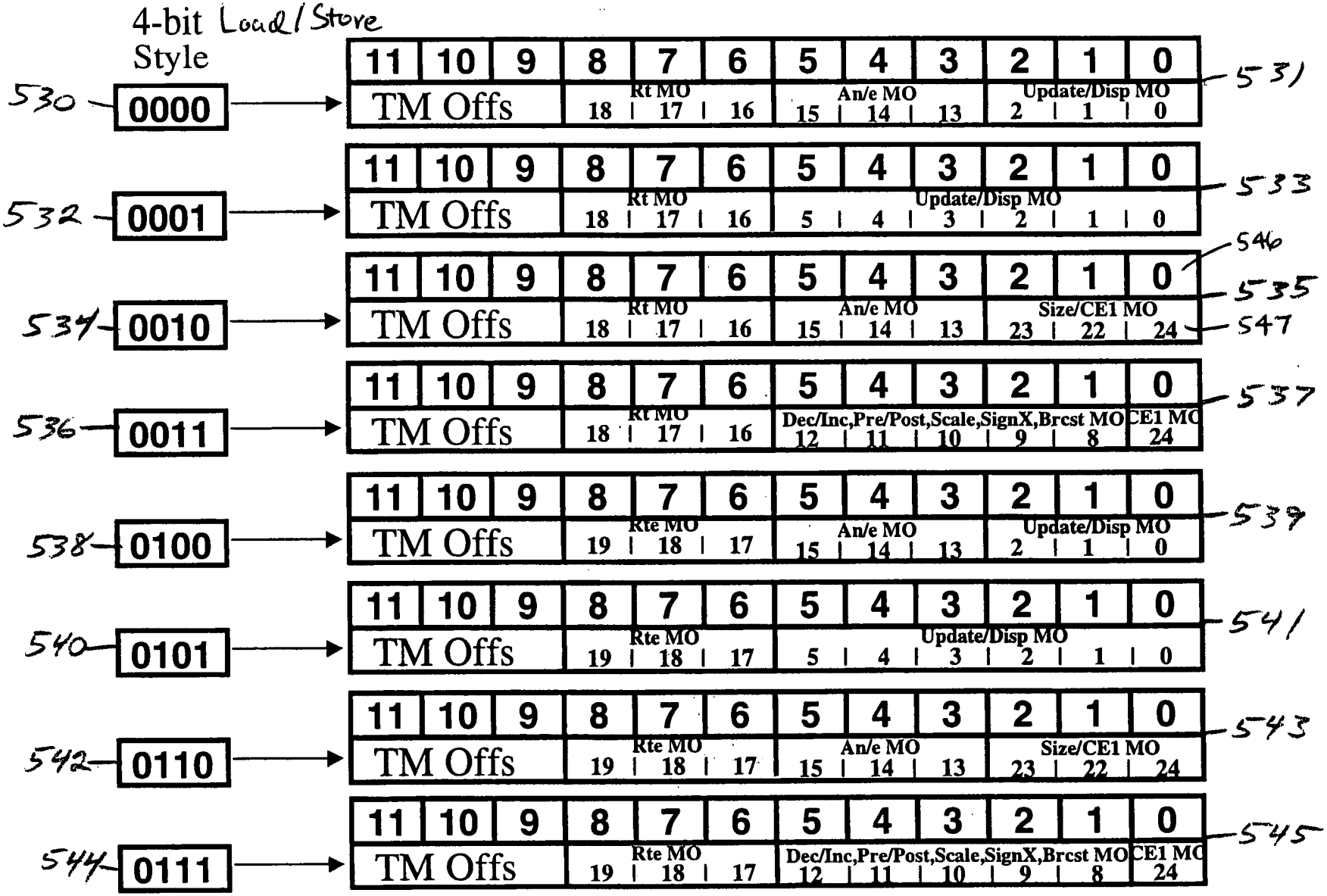
4-bit Load/Store Style
530
0000
TM Offs
11 10 9 8 7 6 5 4 3 2 1 0
Rt MO 18 17 16
An/e MO 15 14 13
Update/Disp MO 2 1 0
531
532
0001
TM Offs
Rt MO 18 17 16
Update/Disp MO 5 4 3 2 1 0
533
534
0010
TM Offs
Rt MO 18 17 16
An/e MO 15 14 13
Size/CE1 MO 23 22 24
546
535
547
536
0011
TM Offs
Rt MO 18 17 16
Dec/Inc,Pre/Post,Scale,SignX,Brcst MO 12 11 10 9 8
CE1 MO 24
537
538
0100
TM Offs
Rte MO 19 18 17
An/e MO 15 14 13
Update/Disp MO 2 1 0
539
540
0101
TM Offs
Rte MO 19 18 17
Update/Disp MO 5 4 3 2 1 0
541
542
0110
TM Offs
Rte MO 19 18 17
An/e MO 15 14 13
Size/CE1 MO 23 22 24
543
544
0111
TM Offs
Rte MO 19 18 17
Dec/Inc,Pre/Post,Scale,SignX,Brcst MO 12 11 10 9 8
CE1 MO 24
545

FIG. 5B

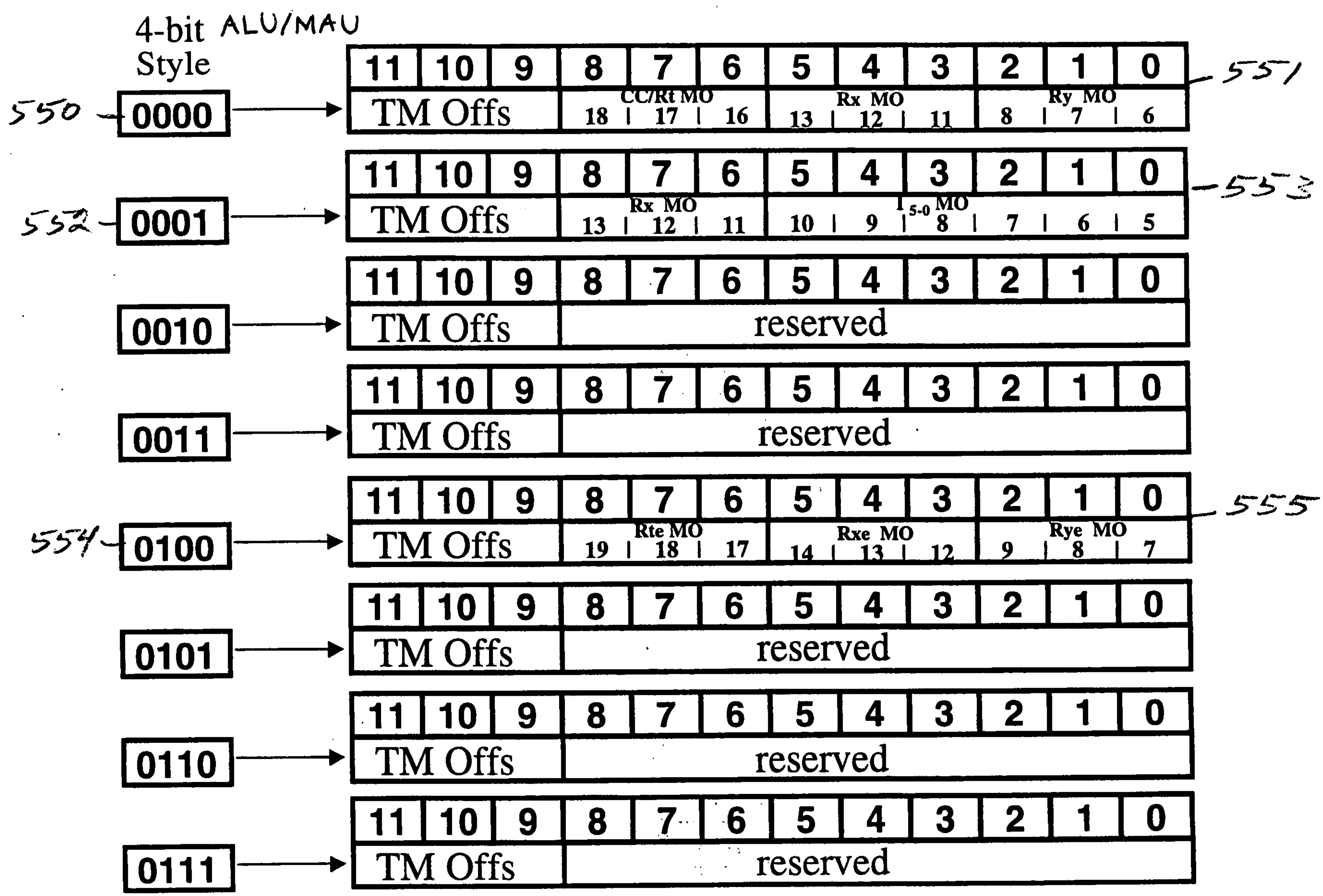
4-bit ALU/MAU Style
550
0000
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
CC/Rt MO
18 17 16
Rx MO
13 12 11
Ry MO
8 7 6
551
552
0001
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rx MO
13 12 11
I5-0 MO
10 9 8 7 6 5
553
0010
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
reserved
0011
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
reserved
554
0100
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rte MO
19 18 17
Rxe MO
14 13 12
Rye MO
9 8 7
555
0101
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
reserved
0110
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
reserved
0111
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
reserved

FIG. 5C

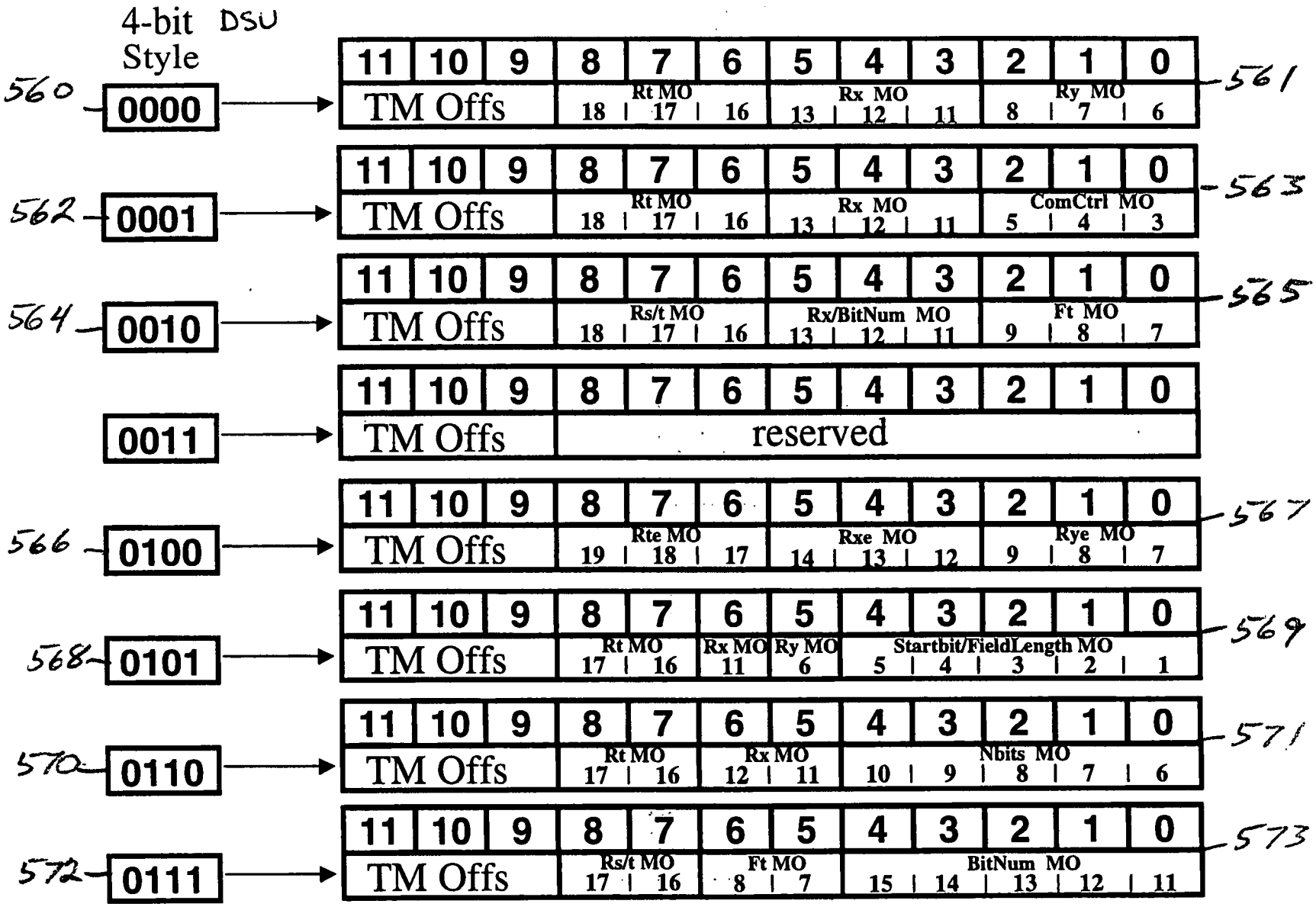
4-bit DSU Style
560
0000
TM Offs
11 10 9 8 7 6 5 4 3 2 1 0
Rt MO 18 17 16
Rx MO 13 12 11
Ry MO 8 7 6
561
562
0001
TM Offs
Rt MO 18 17 16
Rx MO 13 12 11
ComCtrl MO 5 4 3
563
564
0010
TM Offs
Rs/t MO 18 17 16
Rx/BitNum MO 13 12 11
Ft MO 9 8 7
565
0011
TM Offs
reserved
566
0100
TM Offs
Rte MO 19 18 17
Rxe MO 14 13 12
Rye MO 9 8 7
567
568
0101
TM Offs
Rt MO 17 16
Rx MO 11
Ry MO 6
Startbit/FieldLength MO 5 4 3 2 1
569
570
0110
TM Offs
Rt MO 17 16
Rx MO 12 11
Nbits MO 10 9 8 7 6
571
572
0111
TM Offs
Rs/t MO 17 16
Ft MO 8 7
BitNum MO 15 14 13 12 11
573

FIG. 5D

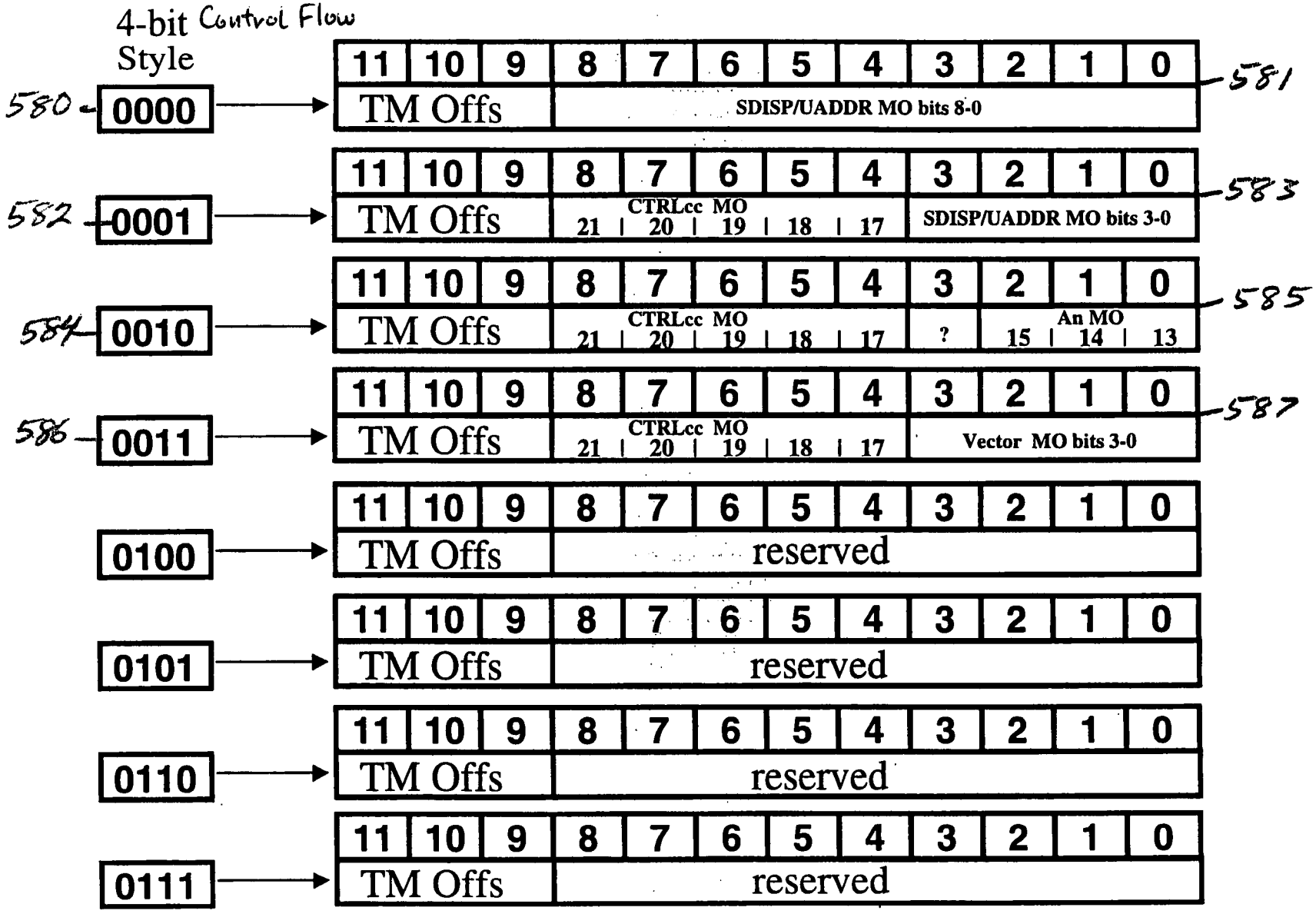
4-bit Control Flow Style
580
0000
TM Offs
SDISP/UADDR MO bits 8-0
581
582
0001
TM Offs
CTRLcc MO 21 20 19 18 17
SDISP/UADDR MO bits 3-0
583
584
0010
TM Offs
CTRLcc MO 21 20 19 18 17
? An MO 15 14 13
585
586
0011
TM Offs
CTRLcc MO 21 20 19 18 17
Vector MO bits 3-0
587
0100
TM Offs
reserved
0101
TM Offs
reserved
0110
TM Offs
reserved
0111
TM Offs
reserved

FIG. 5E

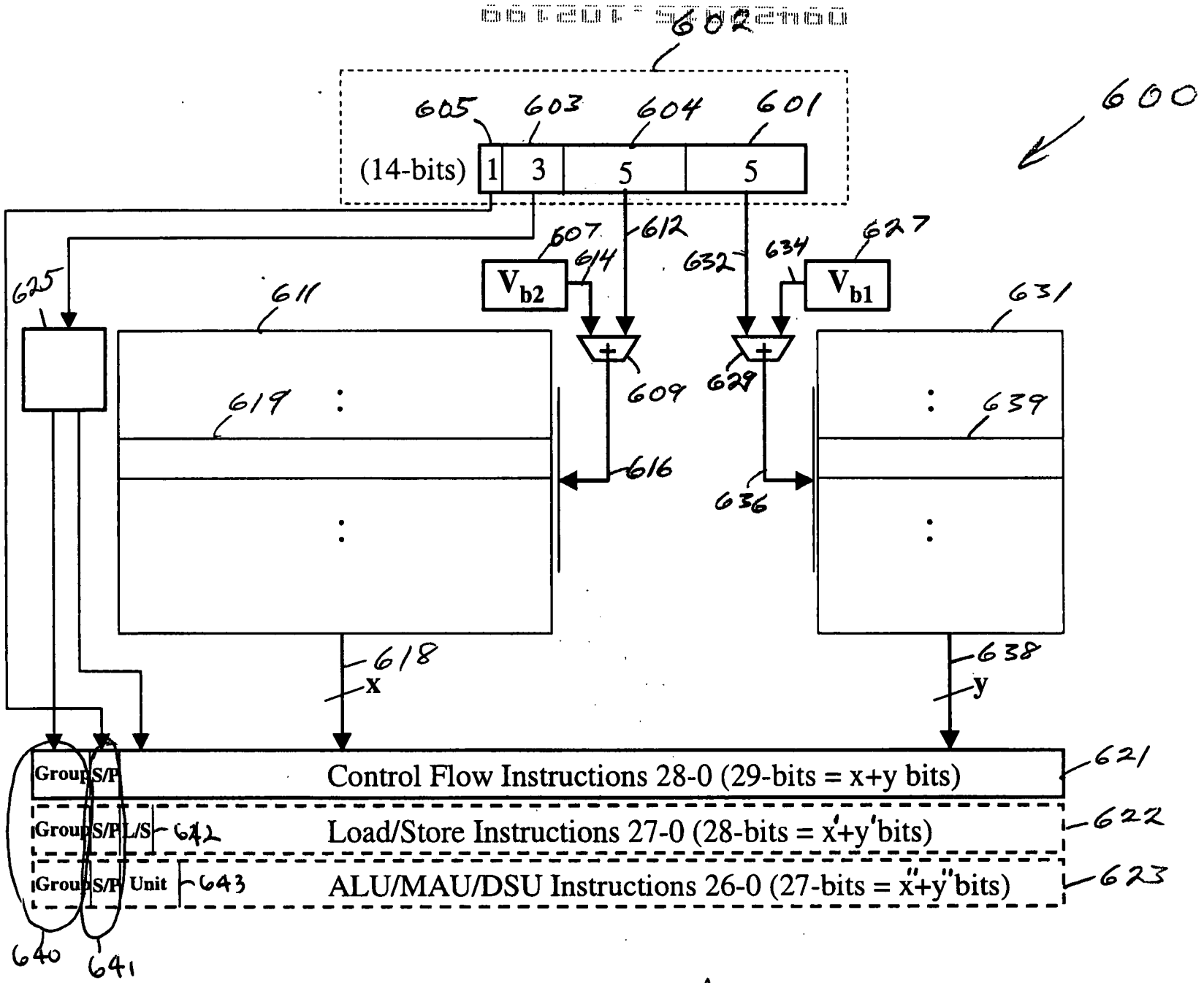
602
600
605
603
604
601
(14-bits)
1
3
5
5
607
612
632
634
627
614
V_{b2}
V_{b1}
625
611
631
609
629
619
639
616
636
618
638
x
y
Group S/P
Control Flow Instructions 28-0 (29-bits = x+y bits)
621
Group S/P L/S
642
Load/Store Instructions 27-0 (28-bits = x'+y'bits)
622
Group S/P Unit
643
ALU/MAU/DSU Instructions 26-0 (27-bits = x"+y"bits)
623
640
641

Fig. 6A

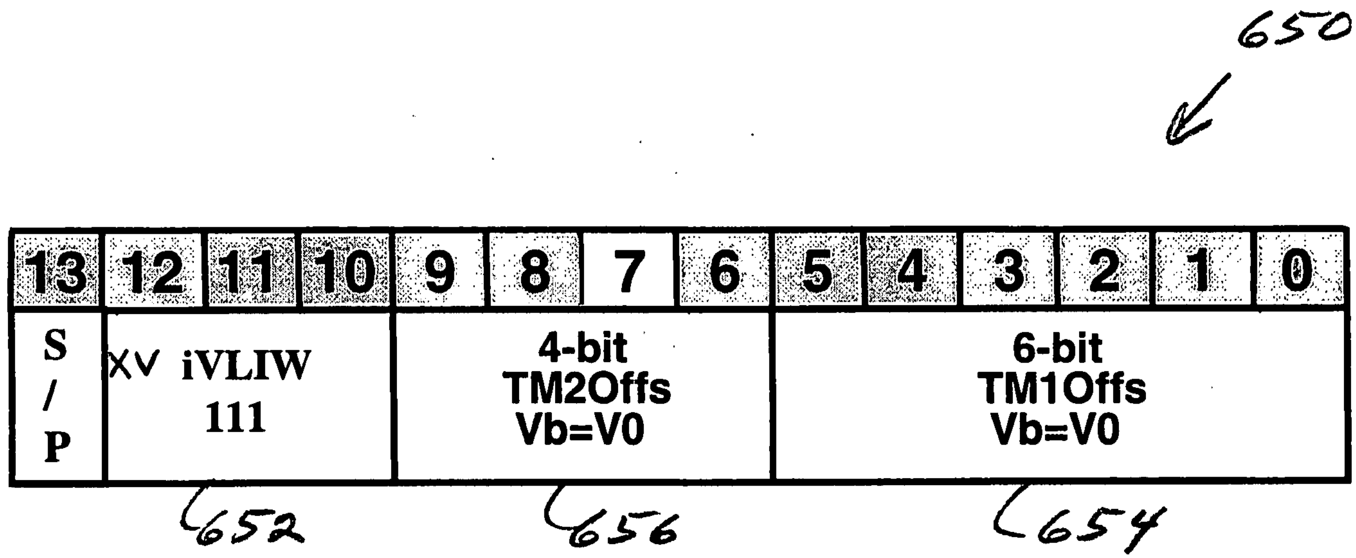
650
13
12
11
10
9
8
7
6
5
4
3
2
1
0
S / P
XV iVLIW 111
4-bit TM2Offs Vb=V0
6-bit TM1Offs Vb=V0
652
656
654

FIG. 6B

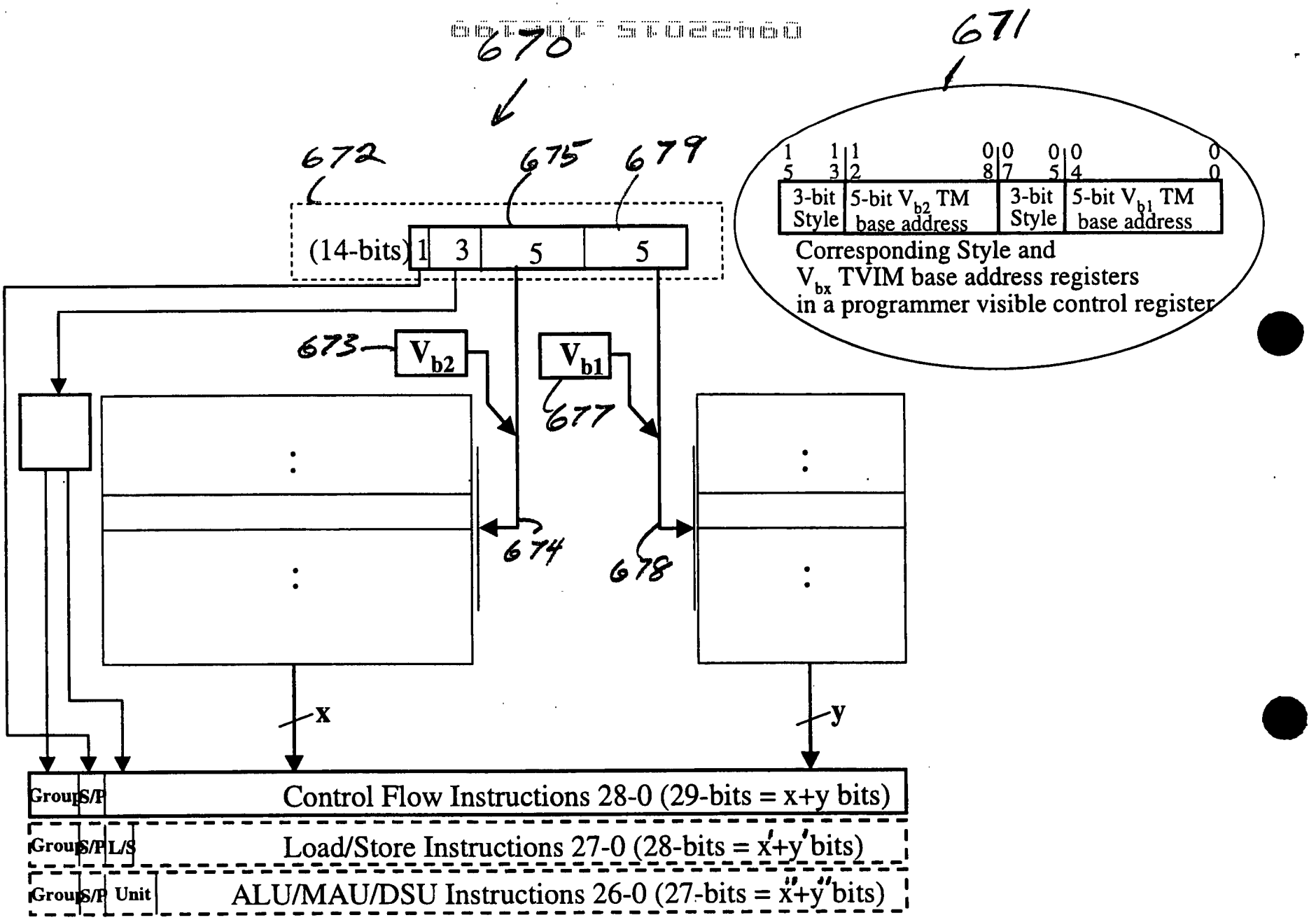
670
671
672
675
679
(14-bits)
1
3
5
5
673
V_{b2}
V_{b1}
677
674
678
x
y
Group
S/P
Control Flow Instructions 28-0 (29-bits = x+y bits)
Group
S/P
L/S
Load/Store Instructions 27-0 (28-bits = x'+y' bits)
Group
S/P
Unit
ALU/MAU/DSU Instructions 26-0 (27-bits = x"+y" bits)
15 13 12 8 7 5 4 0
3-bit Style
5-bit V_{b2} TM base address
3-bit Style
5-bit V_{b1} TM base address
Corresponding Style and
V_{bx} TVIM base address registers
in a programmer visible control register

Fig. 6C

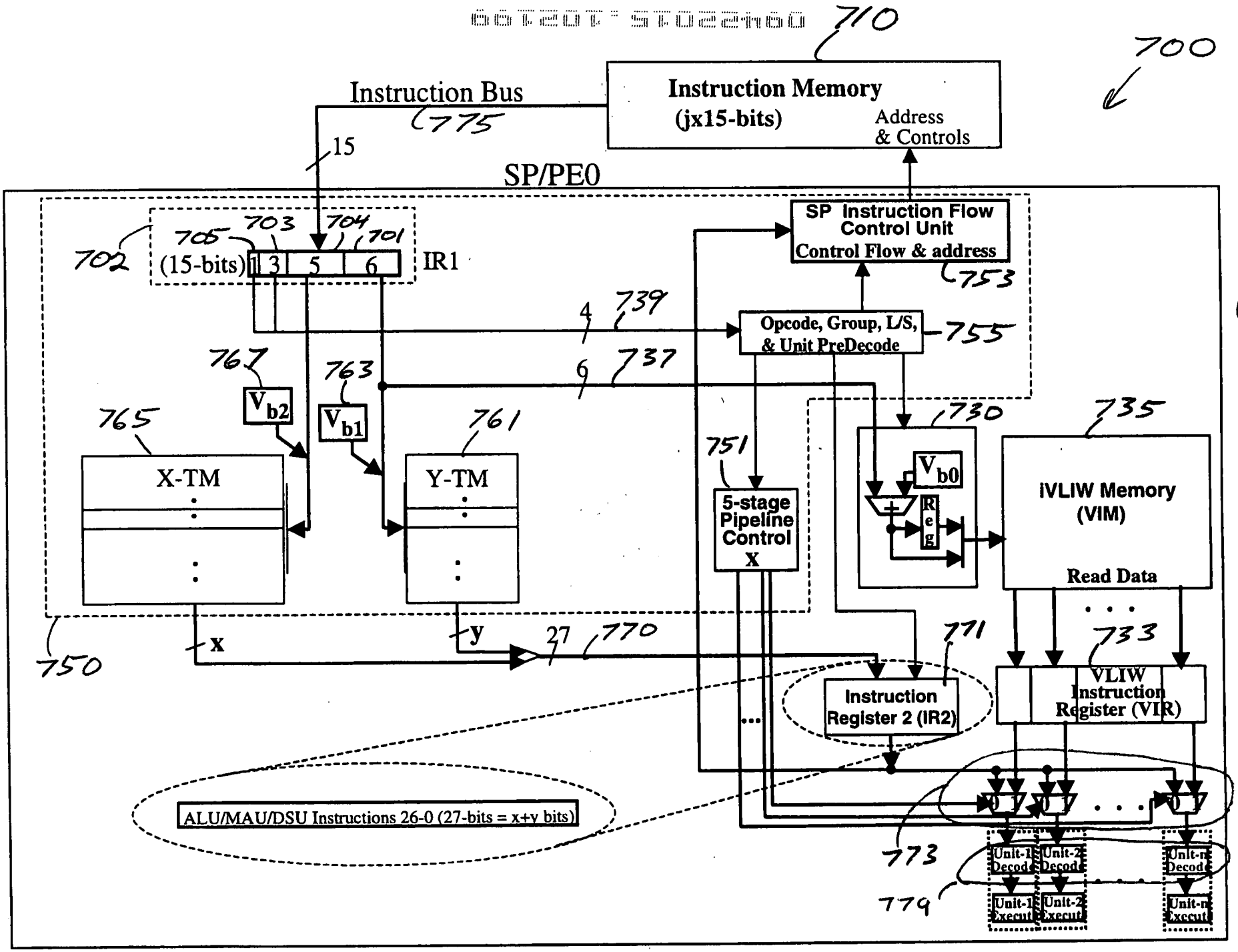
710
700
Instruction Bus
775
Instruction Memory
(jx15-bits)
Address
& Controls
15
SP/PE0
702
705
703
704
701
(15-bits)
1
3
5
6
IR1
SP Instruction Flow
Control Unit
Control Flow & address
753
739
4
Opcode, Group, L/S,
& Unit PreDecode
755
737
6
767
763
V_{b2}
V_{b1}
765
761
751
730
735
X-TM
Y-TM
5-stage
Pipeline
Control
x
V_{b0}
Reg
iVLIW Memory
(VIM)
Read Data
750
x
y
27
770
771
733
Instruction
Register 2 (IR2)
VLIW
Instruction
Register (VIR)
ALU/MAU/DSU Instructions 26-0 (27-bits = x+y bits)
773
779
Unit-1
Decode
Unit-2
Decode
Unit-n
Decode
Unit-1
Execute
Unit-2
Execute
Unit-n
Execute

FIG. 7

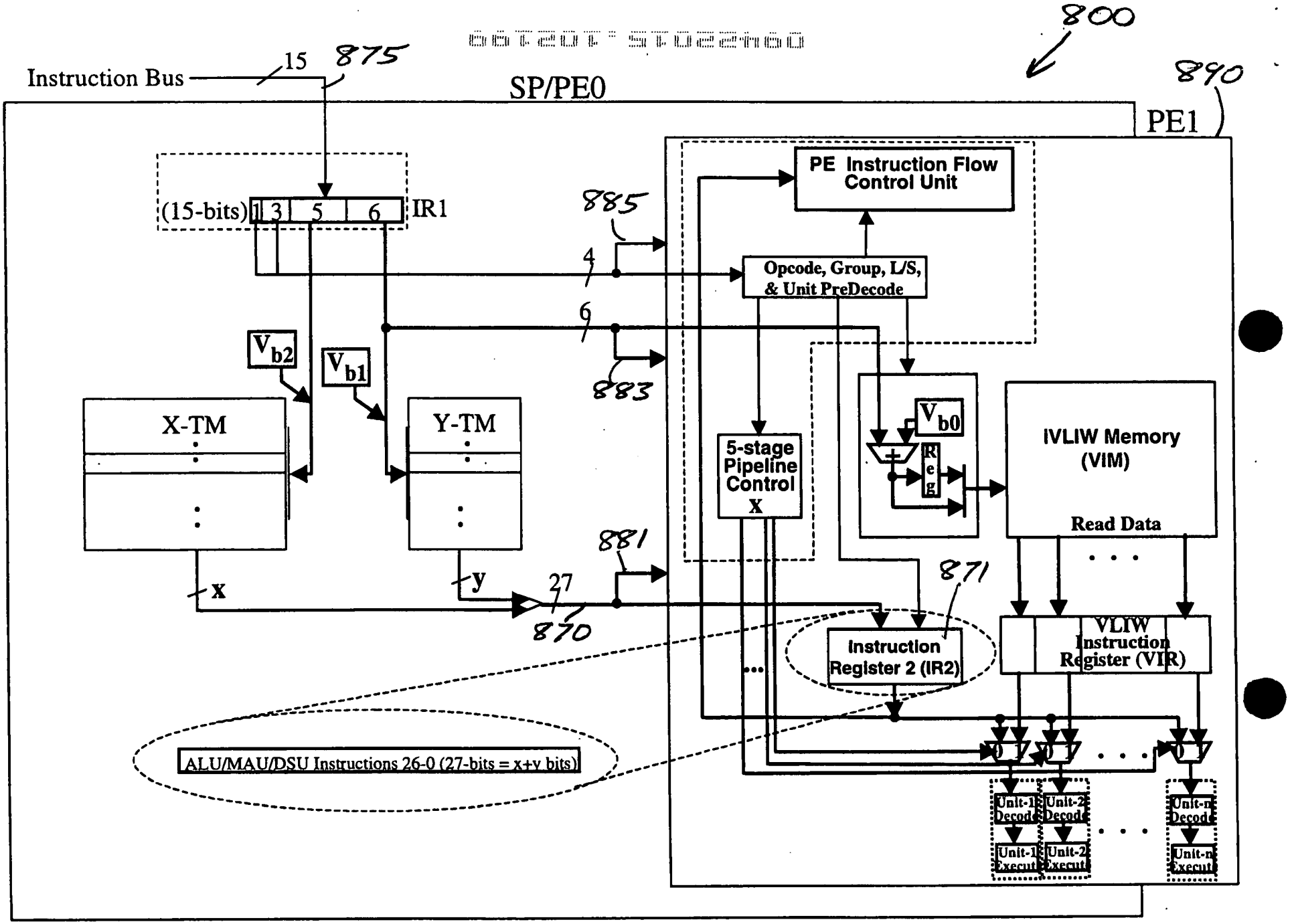
800
Instruction Bus
15
875
SP/PE0
890
PE1
(15-bits)
1
3
5
6
IR1
885
PE Instruction Flow Control Unit
4
Opcode, Group, L/S, & Unit PreDecode
6
883
Vb2
Vb1
X-TM
Y-TM
5-stage Pipeline Control x
Vb0
Reg
IVLIW Memory (VIM)
Read Data
881
871
x
y
27
870
Instruction Register 2 (IR2)
VLIW Instruction Register (VIR)
ALU/MAU/DSU Instructions 26-0 (27-bits = x+y bits)
Unit-1 Decode
Unit-2 Decode
Unit-n Decode
Unit-1 Execute
Unit-2 Execute
Unit-n Execute

FIG. 8

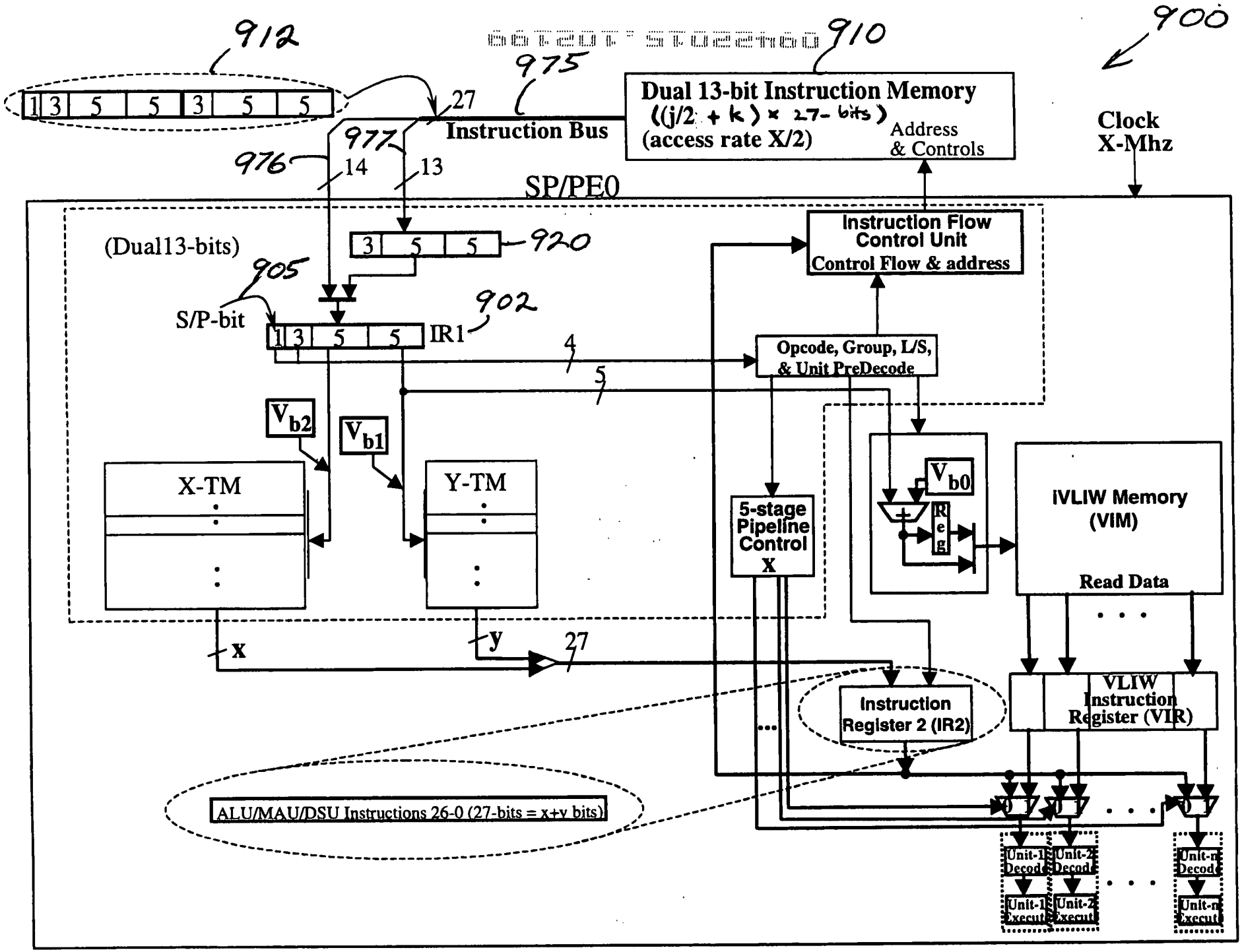
912
910
900
975
Dual 13-bit Instruction Memory
((j/2 + k) x 27- bits)
(access rate X/2)
Address
& Controls
Clock
X-Mhz
27
Instruction Bus
977
976
14
13
SP/PE0
(Dual13-bits)
920
905
S/P-bit
902
IR1
Instruction Flow
Control Unit
Control Flow & address
Opcode, Group, L/S,
& Unit PreDecode
4
5
Vb2
Vb1
Vb0
X-TM
Y-TM
5-stage
Pipeline
Control
x
IVLIW Memory
(VIM)
Read Data
x
y
27
Instruction
Register 2 (IR2)
VLIW
Instruction
Register (VIR)
ALU/MAU/DSU Instructions 26-0 (27-bits = x+y bits)
Unit-1
Decode
Unit-2
Decode
Unit-n
Decode
Unit-1
Execute
Unit-2
Execute
Unit-n
Execute

FIG. 9

1000

	1015 Cycle	1025 Fetch	1035 Xpand & Dispatch	1045 Decode	1055 Execute	1065 Cond. Ret
1010	i	SP Fetches a B-bit Instr(i)= ADD.S instruction & loads it into IR1	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)	Previous Instruction Instr(i-4)
1020	i+1	SP Fetches a B-bit Instr(i+1)=XV.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i)=ADD.S instruction is loaded into IR2. The S/P-bit and 3-bit opcode are decoded in the SP.	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)
1030	i+2	SP Fetches a B-bit Instr(i+2)=COPY.S instruction & loads it into IR1	S/P-bit & opcode indicate an SP XV operation. Local TM fetches occur and a native form of the Instr(i+1)=XV.S instruction is loaded into IR2. The S/P-bit, and 3-bit opcode are decoded in the SP. TheVIM address is calculated and the iVLIW is fetched from the XV VIM	The ALU decodes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)
1040	i+3	SP Fetches a B-bit Instr(i+3)=ADD.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+2)=COPY.S instruction is loaded into IR2.	Instr(i+1)=XV.S causes up to 5 instructions in iVLIW decode	The ALU executes Instr(i)=ADD.S instruction.	Previous Instruction Instr(i-1)
1050	i+4	Fetch next B-bit instruction: Instr(i+4)	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+3)=ADD.S instruction is loaded into IR2.	The DSU decodes the Instr(i+2)=COPY.S instruction	Instr(i+1)=XV.S causes up to 5 instructions in iVLIW execute	The Instr(i)=ADD.S side effects are set in ASFs and ACFs

FIG. 10